NISTIR 4352

NEW NIST PUBLICATION
December 1990

MIS CAPACITOR STUDIES ON SILICON CARBIDE SINGLE CRYSTALS: FINAL REPORT FOR MAY 8, 1989 TO NOVEMBER 8, 1989

J. J. Kopanski

U.S. DEPARTMENT OF COMMERCE
National Institute of Standards
and Technology
Center for Electronics and Electrical
Engineering
Semiconductor Electronics Division
Gaithersburg, MD 20899

Prepared for
National Aeronautics and Space
Administration (NASA)
Cleveland, Ohio

U.S. DEPARTMENT OF COMMERCE
Robert A. Mosbacher, Secretary

NATIONAL INSTITUTE OF STANDARDS
AND TECHNOLOGY
John W. Lyons, Director

NIST

NISTIR 4352

MIS CAPACITOR STUDIES ON SILICON CARBIDE SINGLE CRYSTALS: FINAL REPORT FOR MAY 8, 1989 TO NOVEMBER 8, 1989

J. J. Kopanski

U.S. DEPARTMENT OF COMMERCE
National Institute of Standards and Technology
Center for Electronics and Electrical Engineering
Semiconductor Electronics Division
Gaithersburg, MD 20899

Prepared for
National Aeronautics and Space Administration (NASA)
Cleveland, Ohio

July 1990

U.S. DEPARTMENT OF COMMERCE
Robert A. Mosbacher, Secretary
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
John W. Lyons, Director

Table of Contents

Page

Abstract 1

1. Introduction 3

2. Summary of Previous Work 3

3. Capacitance-Voltage and Conductance-Voltage Measurements 5

   3.1 Conductance-Voltage Behavior 5
   3.2 Voltage Stress Behavior and Bulk Oxide Trapped Charge 7
   3.3 Mobile Ionic Charge 12
   3.4 Effect of Temperature on MIS Capacitor Characteristics 13

4. Current-Voltage Measurements 17

   4.1 Current-Voltage Characteristics 17
   4.2 Insulator Breakdown Field and Resistivity 19
   4.3 Fowler-Nordheim Tunneling and Determination of the $SiC-SiO_2$ Barrier Height 21

5. Deep-Level Transient Spectroscopy 27

6. Conclusions (Electrical Characteristics of SiC MIS Capacitors) 29

Acknowledgments 32

References 33

List of Tables

1. Typical measured charge densities of SiC MIS capacitors 11

2. Typical measured breakdown fields of insulating layers in SiC MIS capacitors 20

List of Figures

1. Typical C-V and G-V responses measured at 10 kHz for a SiC MIS capacitor with a thermal oxide insulator showing "slow trapping" instability 8

2. C-V curves of SiC MIS capacitor after bias-temperature stress showing the effect of mobile ionic charge 14

List of Figures (continued)

3. C-V characteristics of a SiC MIS capacitor at room temperature, 23 °C; 115 °C; 175 °C; and 260 °C 15

4. D_{it} vs. temperature from C-V curves in figure 3 16

5. Typical I-V characteristics for a SiC MIS capacitor in the forward and reverse directions 18

6. Measured current-voltage characteristics of a silicon MOS capacitor . 22

7. Fowler-Nordheim plot of I-V data in figure 6 showing the linear relation between J/F^2 and $1/F$ 23

8. Current-voltage characteristic of an MOS capacitor on as-grown and mechanically polished SiC 24

9. Fowler-Nordheim plot of SiC MIS capacitor I-V data from figure 8 . . . 25

10. DLTS traces for a SiC MIS capacitor with thermal oxide insulator showing the change in shape of the response for four different bias sequences 28

MIS Capacitor Studies on Silicon Carbide Single Crystals: Final Report for May 8, 1989 to November 8, 1989

J. J. Kopanski
Semiconductor Electronics Division
National Institute of Standards and Technology
Gaithersburg, MD 20899

Abstract

In this continuation of previous work, cubic SiC metal-insulator-semiconductor (MIS) capacitors with thermally grown or chemical-vapor-deposited (CVD) insulators were characterized by capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) measurements. The purpose of these measurements was to determine the four charge densities commonly present in an MIS capacitor (oxide fixed charge, N_f; interface trap level density, D_{it}; oxide trapped charge, N_{ot}; and mobile ionic charge, N_m) and to determine the stability of the device properties with electric-field stress and temperature. It was found that an electric-field stress would alter the shape of the SiC MIS capacitor C-V characteristics. A negative voltage stress at room temperature would result in a negative shift of the C-V characteristics, indicating the creation of positive charge in the oxide. A positive voltage stress at room temperature resulted in no detectable shift of the C-V curve. The sense of these shifts in the C-V curves is the same as that observed for the "slow trapping" instability often observed in silicon and other semiconductor-based MIS capacitors. From the shift in the C-V characteristics at the mid-gap point, it was found that a negative voltage stress could increase N_{ot} by as much as 5×10^{11} cm^{-2}. A voltage stress was also found to increase D_{it} by as much as 25%. The mobile ionic charge density was determined from a series of elevated temperature bias stress measurements. N_m for the capacitors in this study ranged from less than 1×10^{11} to 4×10^{11} cm^{-2}. It was found that increasing the temperature would also change the shape of the C-V characteristics, indicating an increase in the number of active interface traps. The resistivity and breakdown field of various insulators on SiC were determined from the I-V characteristics of the capacitors. For capacitors with thermal oxide insulating layers, the average resistivity was about 10^{16} Ω-cm, and the average electric breakdown field was 3.3×10^6 V/cm. Fowler-Nordheim tunneling was identified as the charge conduction mechanism of thermal oxide layers on cubic SiC. The barrier height between n-type SiC and SiO_2 for the tunneling of electrons was determined to be 2.9 eV with an electron effective mass of 0.5 by fitting the Fowler-Nordheim formula to the observed I-V curve. Finally, some deep-level transient capacitance measurements were attempted on some of the SiC MIS capacitors and on Au on SiC Schottky diodes. In the conclusions of this report, a comprehensive summary of the electrical properties of cubic SiC MIS capacitors is presented.

Key Words: capacitance-voltage measurements; charge injection; conductance-voltage measurements; Fowler-Nordheim tunneling; high temperature electronics; interface traps; MIS capacitor; MOS capacitor stability; oxide traps; semiconductors; silicon carbide; slow trapping instability.

Disclaimer

Certain commercial equipment, instruments, or materials are identified in this report in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

1. INTRODUCTION

The work described in this report was done for the National Aeronautics and Space Administration (NASA), Lewis Research Center, under NASA Lewis Order No. C-30018-M, for the period May 8, 1989 to November 8, 1989. The program is entitled "MIS Capacitor Studies on Cubic Silicon Carbide Single Crystals" and is a continuation of activities initiated under NASA Lewis Order No. C-30007-K in February 1988.

Silicon carbide (SiC) is a semiconductor with several attractive properties for electronic devices. These include a large band gap (2.2 eV in cubic SiC), high thermal conductivity, and high breakdown field, as well as excellent physical stability. Due to these electronic and physical properties, silicon carbide has long been known as an attractive material for high-temperature, high-frequency, and high-power electronic devices. SiC-based electronics have potential aerospace and space applications.

The development of SiC electronics has been spurred by progress in crystal growth technology. One promising technique is the growth of single-crystal layers of the cubic (3C) form of SiC on silicon substrates by chemical-vapor deposition (CVD) processes [1]. The SiC used in this work was grown by this technique. The growth of bulk crystals of a hexagonal (6H) polytype by the seeded sublimation technique has also been improved upon recently and is progressing towards 2-in. diameter wafers [2]. Application of the CVD growth technology originally developed to grow 3C SiC on Si has been applied to the growth of extremely high-quality layers of 3C and 6H SiC on the bulk 6H SiC wafers [3].

SiC metal-oxide-semiconductor field-effect-transistors (MOSFETs) operating at temperatures as high as 650 °C have been reported from several sources [4-7]. A crucial component of MOSFETs is the MOS capacitor which is used to control the conductivity of the channel between the oppositely doped source/drain regions. MOS capacitors on both cubic [8-12] and hexagonal [13-14] SiC have been reported. These reports dealt with a limited number of oxidation conditions and devices and were primarily to demonstrate that unpinned MOS capacitors on SiC could be made to invert the conductivity type of the underlying SiC.

In the work reported here and in the previous report [15], detailed electrical characterization and optimization of the fabrication processes of metal-insulator-semiconductor (MIS) capacitors on SiC are described. Analysis of the electrical characteristics yields information about the properties of the insulator-SiC interface and the SiC. If devices incorporating MIS capacitors are to function at high temperature and electric-field stress, their stability with respect to these conditions must be established. Thus, in the work reported here, a further goal was to determine SiC MIS capacitor stability with respect to temperature and electric-field stress.

2. SUMMARY OF PREVIOUS WORK

The previous annual report [15] describes in detail the fabrication of MIS

capacitors on cubic SiC substrates. The insulating layers for these devices were either thermally grown oxides or CVD silicon dioxide layers. The effect of various processing conditions on the resulting device electrical properties was investigated.

For thermal oxide layers, the effects of oxidation time, temperature, and oxidation gasses on the electrical properties of the capacitors were determined. It was found that the capacitor electrical characteristics were relatively independent of oxidation temperature and that wet oxidation produced capacitors with much lower fixed charge density than dry oxidation.

For CVD oxide layers, the effect of various post-deposition thermal treatments was determined. It was found that a three-step process (consisting of a densification step in nitrogen between 1100 and 1150 °C, a short, wet oxidation step immediately following, and a micro-alloying step in 10% hydrogen, 90% nitrogen forming gas after aluminum metal deposition) produced an MIS capacitor with properties similar to those with an insulating layer consisting completely of thermal oxide.

The devices fabricated were originally electrically characterized from their ac capacitance-voltage (C-V) behavior [15]. The ac measurement frequency was between 100 Hz and 4 MHz. The C-V behavior was also measured at temperatures between 25 and 300 °C. The measurement of the capacitor C-V characteristics was used to quickly show that a device displayed the desired accumulation, depletion, and inversion regions of operation.

Basic interpretation of the C-V characteristics yielded the oxide thickness, T_{ox}; the SiC substrate doping density, N_d; the capacitor flatband voltage, V_{fb}; and the oxide fixed charge density, N_f. It was found that N_f for these SiC MIS capacitors was between 5 and 9 x 10^{11} cm^{-2}. In addition, the interface trap level density, D_{it}, was determined as a function of energy in the bandgap. D_{it} was determined by the Terman method [16], which involves comparing the measured high-frequency C-V curve to a theoretical curve. It was found that D_{it} at mid-gap was between 0.5 and 2.0 x 10^{11} cm^{-2} eV^{-1} and that a peak in D_{it} several times greater than the mid-gap level was present at about 0.6 eV below the conduction band edge.

The research reported here is an expansion of the electrical characterization begun during the previous contract. A goal was to characterize completely all the charges present in a SiC MIS capacitor: the oxide fixed charge density, N_f, the interface trap level density, D_{it}, the oxide trapped charge density, N_{ot}, and the mobile ionic charge density, N_m. Knowledge of the charge components present in SiC MIS capacitors allows the prediction of the eventual operating properties of MOSFETs fabricated with SiC.

It had previously been observed that a large electric field could result in a shift in voltage and a change in shape of the C-V characteristics of a SiC MIS capacitor [15]. This type of behavior indicates that bulk oxide and interface trapped charges were being created or charged by the voltage stress. The changes in an MIS capacitor's C-V characteristics at the flatband, mid-gap, and inversion points following a voltage stress were used to separate the effects due to changes in interface trap density, D_{it}, and bulk traps,

N_{ot} [17]. Additional information on N_{ot} was obtained from monitoring the change in the conductance vs. voltage (G-V) characteristics following a voltage stress.

The C-V behavior was also measured as a function of temperature. These measurements determined the mobile ionic charge density, N_m, by the bias-temperature drift technique [18]. The effect of temperature on the apparent D_{it} profile was also quantified.

The current vs. voltage (I-V) characteristics of the SiC MIS capacitors were also determined. These measurements allowed the precise determination of the oxide breakdown field, E_{bd}, and resistivity, ρ. A linear $\log(J/F^2)$ vs. $1/F$ dependence was seen (where J is the current density and F is the electric field) for conduction in SiC MIS capacitors. As with silicon MOS capacitors, this implies that the charge conduction mechanism in the oxide is due to Fowler-Nordheim (F-N) tunneling [19]. Interpretation of the I-V behavior allowed the determination of the SiC-SiO_2 barrier height.

Finally, some deep-level transient spectroscopy (DLTS) measurements were attempted on the MIS capacitors. The primary goal of these measurements was to determine the feasibility of extracting deep-level properties from DLTS measurements on SiC MIS capacitors. Additional measurements were tried on some Au on SiC diodes that were fabricated in an attempt to form Schottky diodes.

3. CAPACITANCE-VOLTAGE AND CONDUCTANCE-VOLTAGE MEASUREMENTS

3.1 Conductance-Voltage Behavior

Carrier traps at the semiconductor-insulator interface result in an admittance (capacitance and conductance) in parallel with the capacitance due to the oxide layer and depletion region of an MIS capacitor. In general, the existence of interface trap levels will result in a peak in the G-V behavior. The height of this peak can be related to the interface trap density at a surface potential, ψ_S, corresponding to the applied voltage at which the peak occurs. The conductance due to interface traps is not measured directly, but is extracted from the measured conductance using an equivalent circuit. Knowing the conductance of an MIS capacitor as a function of voltage and at many ac measurement frequencies, ω, detailed information about the interface trap level density, capture probability and time constant dispersion can be determined [20].

Extensive measurements of the G-V response at various ω's are necessary for a comprehensive study of interface traps. G-V measurements were carried out here at only a few frequencies. These measurements were to determine that the general G-V behavior of SiC MIS capacitors was as predicted and that D_{it} determined from the conductance method at a few points in ψ_S was in agreement with D_{it} determined from the Terman method.

The equivalent parallel conductance of the SiC MIS capacitors was measured using Hewlett-Packard 4274A and 4275A multi-frequency LCR meters. The

measured C-V and G-V behavior was corrected for the series resistance of the devices. From the peak value and location in voltage of the corrected G-V curve, the value of D_{it} at the corresponding ψ_S was determined.

A real MIS capacitor has a series resistance, R_S, associated with it due to the contact resistance of the metal contact and the resistivity of the semiconductor. R_S can be dependent on the measurement frequency. For the SiC MIS capacitors used in this study, R_S had a significant effect on the measured C-V and G-V characteristics above about 100 kHz. The series resistance was determined from the conductance, G_{ma}, and capacitance, C_{ma} of the capacitors when biased in strong accumulation [21]:

$$R_S = G_{ma}/(G_{ma}^2 + \omega^2 C_{ma}^2). \quad (1)$$

The corrected capacitance and parallel conductance were calculated from the measured values and the series resistance. The corrected G and C values were used for all calculations. R_S for the SiC capacitors used in this study varied between about 80 and 500 Ω, depending on the SiC resistivity.

Most simply, the SiC capacitors in depletion can be modeled by an equivalent circuit consisting of the oxide capacitance, C_{ox}, in series with the depletion capacitance, C_D, with an admittance due to interface traps, Y_{it}, in parallel to C_D [22]. The interface trap admittance consists of an interface trap capacitance component, $C_{it}(\omega)$, and an equivalent parallel conductance component, $G_p(\omega)$.

The equivalent circuit is extended to include the effects of time constant dispersion caused by the distribution in energy of interface trap levels and effects due to the random spatial distribution of discrete interface charges [23]. These effects tend to broaden the peak in the G_p vs. voltage response. The equivalent parallel conductance averaged over these two effects is denoted as $\langle G_p \rangle$. In terms of the measured capacitance and conductance, $\langle G_p \rangle$ is given as [24]:

$$\langle G_p \rangle/\omega = (\omega C_{ox}^2 G_m)/(G_m^2 + \omega^2 (C_{ox} - C_m)^2) \quad (2)$$

where G_m is the measured equivalent parallel conductance, C_{ox} is the oxide capacitance, and C_m, the measured capacitance (all corrected for series resistance).

The interface trap level density was related to the peak value of $\langle G_p \rangle/\omega$ from the condition: $G_p/(\omega C_{it}) = G_p/(\omega q D_{it}) = 0.5$ for a single level of interface traps. For a distribution of interface traps, D_{it}, was determined as [25]:

$$D_{it} = (\langle G_p \rangle/\omega)_{peak}/0.4q \quad (3)$$

where $(\langle G_p \rangle/\omega)_{peak}$ is the peak in $\langle G_p/\omega \rangle$ plotted vs. voltage. This provides a measure of D_{it} at one value of surface potential. The value of ψ_S corresponding to the applied gate voltage was determined in the same manner as for the Terman method [15-16].

Typical C-V and G-V responses measured at 10 kHz for a SiC MIS capacitor are shown as figure 1. The G-V behavior of SiC MIS capacitors was found to be very similar to that commonly seen for silicon MOS capacitors. A sharp peak is seen in the measured G-V characteristics. The measured G_p was found to be approximately proportional to measurement frequency for 1 kHz $\leq \omega \leq$ 4 MHz. The correction of the measured C and G for series resistance was small at frequencies less than about 100 kHz. At higher frequencies, the correction for series resistance is progressively larger. Above 1 MHz, the peak in the conductance is obscured without correction for the series resistance. D_{it} determined from the peak in the G-V characteristics agreed within a factor of two with the value determined from the Terman method.

The G-V behavior of SiC MIS capacitors with CVD oxide insulators was very similar to those with thermal oxide insulators. The conductance peaks appeared to be about twice as wide (in voltage) for capacitors with CVD oxide insulators compared to those with thermal oxide insulators. This indicates that the interface trap levels for these devices may have a wider distribution in energy and capture cross section.

As shown in figure 1, a voltage stress was found to change the conductance peak location and height. This is discussed in the next section.

3.2 Voltage Stress Behavior and Bulk Oxide Trapped Charge

It was reported in the previous annual report [15] that a stress voltage applied to a SiC MIS capacitor resulted in a shift of the C-V characteristics with voltage. These changes of the C-V characteristics indicate that SiC MIS devices might have potential long-term stability problems. Such shifts in C-V characteristics indicate that charges have been generated in the insulator by the voltage stress. The charge generated will reside in either interface traps or bulk oxide traps. As the two types of traps affect the C-V characteristics in different ways, the effects due to bulk oxide trapped charge, N_{ot}, and the number of interface trapped charges, N_{it}, can be separated [17].

The effects of voltage stress on the SiC MIS capacitors was quantified by: 1) measuring an initial C-V curve; 2) applying a dc voltage stress for a set time; and 3) measuring the C-V curve again. The voltage sweep range used to acquire C-V data was restricted so that additional shifts in the C-V curve were not caused by the voltage sweep. After measurement of the initial C-V curve, stress voltages of increasing magnitude were applied sequentially. A common sequence was to apply voltage stresses of ±5, 10, 15, and 20 V for 10 min and to measure the C-V curve between each voltage stress. The applied voltage stresses were then converted to the electric field at the semiconductor surface.

Two distinct mechanisms were found that resulted in a shift or distortion of the C-V characteristics after a voltage stress. Trapping in the bulk oxide, which resembled that expected from hole injection from the substrate, was seen at room temperature. This is very similar to the negative bias temperature instability (NBTI) or slow trapping that has been reported for MIS diodes in

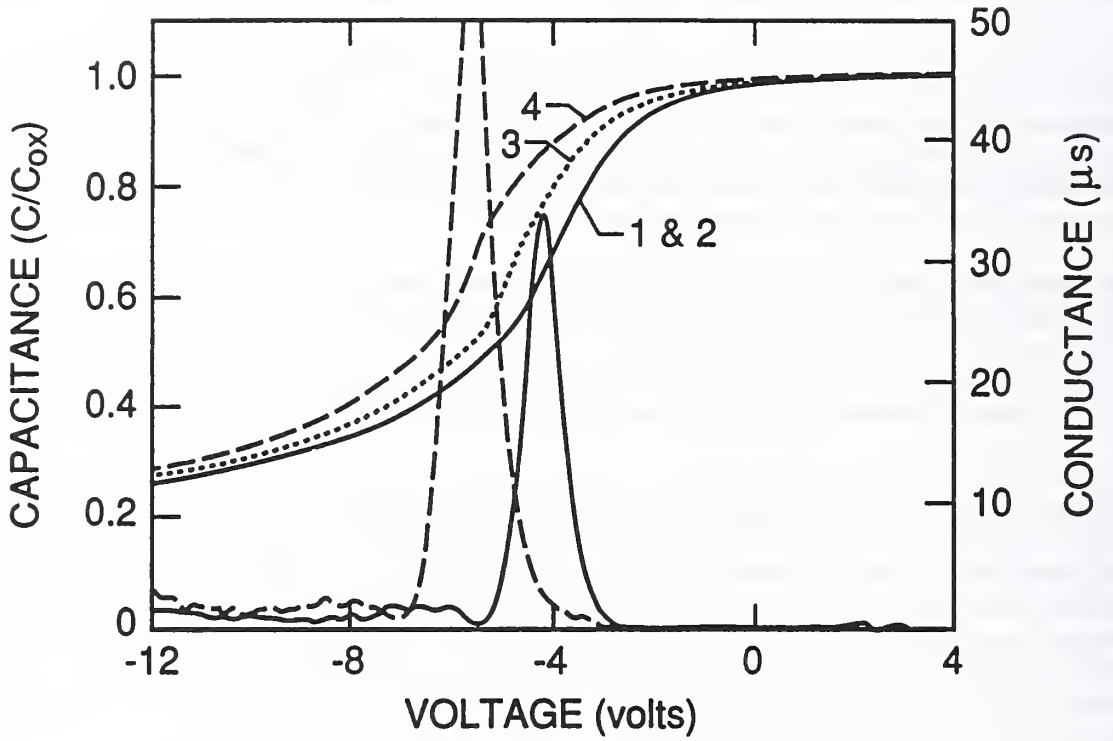

Figure 1. Typical C-V and G-V responses measured at 10 kHz for a SiC MIS capacitor (SiC #820-2) with a thermal oxide insulator showing "slow trapping" instability. 1) Before any voltage stress; 2) after -10 V, 10-min, room-temperature stress; 3) after -15 V stress; 4) after -20 V stress. For this device before any stress, the fixed oxide charge, N_f, was determined to be 7.5 x 10^{11} cm^{-2}, D_{it} at mid-gap was determined to be 1.2 x 10^{11} $cm^{-2}eV^{-1}$. After the final voltage stress, N_{ot}, was seen to have increased to 4.4 x 10^{11} cm^{-2} and D_{it} was increased by about 25 percent.

silicon [26-28], InSb [29], InP [30], and other II-VI and III-V semiconductors. Mobile ionic contamination was identified from elevated temperature positive bias-stress cycles. This is discussed in the next section.

Voltage stresses applied to SiC MIS (both thermal and CVD oxide insulators) capacitors were found to produce the following effects:

1) At room temperature and above a threshold field of about -1.5 x 10^6 V/cm, a negative voltage stress (capacitor biased in depletion) results in a shift of the C-V and G-V curves towards more negative voltages. Typical response for a capacitor with a thermal oxide insulator is shown in figure 1. The direction of the shift in the C-V characteristics indicates that positive charge has been generated within the insulator. The shift in voltage of the peak in the G-V curve indicates that bulk oxide traps have been charged. The peak height also increases with stress, indicating an increase in interface trap level density. This type of stress-voltage-induced shift is responsible for the hysteresis between the forward and reverse voltage sweep C-V curves seen in many SiC MIS capacitors.

The magnitude of the shift increases with more negative stress voltage until the capacitor breakdown voltage is exceeded. The amount of shift due to a stress at a particular voltage saturates a few minutes after applying the voltage. Stress times of 10 min at room temperature were commonly used in experiments and were adequate to produce the maximum shift at that electric field.

2) The shift in device characteristics from a negative voltage stress is "permanent" at room temperatures. The shift can be somewhat reversed by biasing at slightly positive voltages at elevated temperatures. For example, a capacitor with a thermal oxide insulator was subject to a 1-min, room-temperature stress at -16 V, which produced a -0.6 V shift in the C-V curve at the flatband point. A subsequent "discharge" stress of +0.1 V at 200 °C for 10 min reversed 0.4 V of the shift. This partial de-trapping indicates that some of the shift is due to electrons tunneling from neutral traps near the interface into the SiC, leaving behind positive charges [31]. These traps must be very near the SiC-SiO_2 interface for de-trapping to occur.

3) A positive voltage stress (capacitor biased in accumulation) at room temperature does not result in any corresponding shift in the device characteristics. This type of voltage asymmetry has also been observed for slow trapping in silicon and other semiconductor-based MIS capacitors. It is assumed that hole traps near the semiconductor-insulator interface are present at a much larger density than electron traps. A large majority of electrons introduced into the insulator pass through to the opposite electrode without being trapped, while almost all holes become trapped.

4) Voltage stress measurements similar to those performed on thermal oxide SiC capacitors were made on SiC capacitors with CVD oxide dielectrics. The voltage stress behavior of the capacitors with CVD oxide insulators was very similar to that of the thermal oxide capacitors.

Quantitatively, the amount of the shift of the C-V curves due to a change in the oxide trapped charge, Q_{ot}, and the amount due to the interface trapped charge, Q_{it}, can be obtained. The charge components can be deduced from the shift of the C-V curve at flatband, mid-gap, and strong inversion [17,32]. These points correspond to semiconductor surface potential, ψ_s, of 0, ϕ_b, and $2\phi_b$, where ϕ_b is the bulk potential. The net inversion-point shift, ΔV_{net}, can be divided into components resulting from interface states, ΔV_{nit}, and trapped oxide charge, ΔV_{Not}:

$$\Delta V_{net} = \Delta V_{Nit} + \Delta V_{Not}. \qquad (4)$$

If the interface traps in the upper half of the bandgap are predominately acceptors and those in the lower half of the bandgap are predominately donors, then at mid-gap neither acceptor nor donor states are charged. The shift in the C-V curve at mid-gap is then due entirely to trapped oxide charge ($\Delta V_{mg} = \Delta V_{Not}$).

Similarly, the increase in "stretchout" of the C-V curves along the voltage axis from mid-gap to inversion is caused only by changes in occupied interface states in the bandgap between mid-gap and inversion. The change in stretchout yields ΔV_{Nit}. V_{so} is defined as V_g(inversion) - V_g(midgap). The change in stretchout, ΔV_{so}, is the difference between the stretchout in pre- and post-stress C-V curves.

For example, the C-V curves obtained for the thermal oxide capacitor on SiC #820-2 before stress and after -10, -15, and -20 V stresses for 10 min are shown in figure 1. By comparing the C-V curves measured initially and after the -20 V stress, the following voltage shifts at the flatband, ΔV_{fb}, mid-gap, ΔV_{mg}, and inversion, ΔV_{in}, points are seen:

ΔV_{fb} =	-1.2 V		
$\Delta V_{mg} = \Delta V_{Not}$ =	-1.5 V	$\Delta N_{ot} = 4.4 \times 10^{11}$ cm^{-2}	
ΔV_{in} =	-1.6 V		
$\Delta V_{so} = \Delta V_{Nit}$ =	-0.1 V	$\overline{\Delta D_{it}} = 0.7 \times 10^{11}$ cm^{-2} eV^{-1}	(average between mid-gap and inversion)

The shifts in voltage were obtained by determining the capacitance at flatband, C_{fb}, mid-gap, C_{mg}, and inversion, C_{in}, of the initial curve and determining the voltage at which those capacitances occur on the stressed curves. The change in oxide trapped charge, ΔN_{ot}, was obtained from the shift in voltage as $\Delta V_{mg} * C_{ox}/(A*q)$ where A is the capacitor area and q the electron charge. The change in average interface trapped charge, ΔD_{it}, was obtained from the change in stretchout as $\Delta V_{so} * C_{ox}/(A*q)/\phi_b$.

The same information about D_{it} can be obtained from the increase in the height of the peak in the G-V curve. For the same capacitor the conductance peak shifted -1.4 V after the -20 V stress. This shift is attributed almost entirely to oxide trapped charge. The change in interface trapped charge is obtained from the increase of the peak conductance.

ΔV_{peak} = -1.4 V
ΔG_{peak} = +16 μS (@ 10 kHz) $\Delta D_{it} = 1.0 \times 10^{11}$ cm^{-2}eV^{-1} (@ ψ_s = -0.1 eV)

In this case, D_{it} was obtained from the conductance peak height for both the initial and stressed cases via eqs (2) and (3) above. The increase, ΔD_{it}, is the difference between D_{it} obtained for the initial and stressed cases.

A summary of similar voltage stress measurements and analysis for several capacitors with thermal or CVD oxide insulators is included as table 1. The various devices were very similar in their response to a stress field, even though they were fabricated with different processes. The maximum stress field investigated (about 3.0 x 10^6 V/cm) was found to create/charge about 5 x 10^{11} oxide traps per cm^2 and to increase D_{it} by about 25 percent.

TABLE 1 TYPICAL MEASURED CHARGE DENSITIES OF SiC MIS CAPACITORS

SiC ID#	Insulator	Initial			Stress 1		Stress 2	
		N_f	D_{it}	N_m	ΔN_{ot}	ΔD_{it}	ΔN_{ot}	ΔD_{it}
820-2*	1150 °C, thermal	7.5	1.2	2.0	+1.8	+4.4	+4.4	+6.3
977-9	1100 °C, thermal	11.1	1.1	2.1	+2.2	+5.9	+5.3	+10.8
975-5	1050 °C, thermal	8.6	1.2	1.8	+2.3	+5.9	+5.5	+4.1
916-9*	CVD, densified at 1000 °C	12.6	2.6	1.9	+2.7	+1.9	+5.3	+5.7

N_f, N_m, and ΔN_{ot} are in units of x 10^{11} cm^{-2}.
D_{it} is in units of x 10^{11} cm^{-2} eV^{-1} (at mid-gap).
ΔD_{it} is in units of x 10^{10} cm^{-2} eV^{-1}.
* SiC grown on (001) silicon; others were grown on slightly off-axis Si.

Table 1 Typical measured charge densities of SiC MIS capacitors. Stress 1 was at -15 V for 10 min at room temperature (electric field of about 2.3 x 10^6 V/cm). Stress 2 was at -20 V for 10 min at room temperature (electric field of about 3.0 x 10^6 V/cm). The mobile ionic charge density, N_m, was determined from the flatband voltage shift after a stress at +7 V for 20 min at 200 °C.

A negative voltage stress is seen to produce increases in both N_{ot} and N_{it}. The change in both of these quantities may be due to charging of existing traps or creation of new traps. The C-V curve is shifted to more negative voltages, implying that positive charge has been created. Positive charge can be created from holes injected into the oxide from the substrate and sequentially trapped in the oxide. Two issues arise: 1) the mechanism that creates positive charge at high negative fields and 2) the origins of the hole traps.

No single mechanism has been generally agreed upon as that responsible for positive charge creation during a negative electric-field stress of an MIS capacitor. A number of possible mechanisms are discussed in [31]. A common feature of all possible mechanisms is that charge must be created in or injected into the oxide. Carriers may be introduced into the insulator from

the semiconductor or the metal via avalanche injection, Fowler-Nordheim tunneling, or some sort of trap-assisted tunneling. As all these processes result in a similar effect on the MIS capacitor, the exact mechanism or mechanisms cannot be isolated from just the effect of a voltage stress on the SiC MIS capacitors.

The exact electrochemical origin of hole traps in SiO_2 is also unclear. From studies on silicon MOS capacitors, two facts about their nature are clear. Oxides grown in wet oxygen are more susceptible to slow trapping than those grown in dry oxygen [26]. The presence of water in the oxide will increase the amount of slow trapping. In addition, radiation damage, such as that due to reactive ion etching or electron beam metallization, has been reported to increase dramatically the amount of slow trapping that a capacitor exhibits [28]. Hole traps in silicon are generally assumed to be very near the Si-SiO_2 interface.

Determination of the bulk oxide and oxide-semiconductor charge trapping properties via voltage stress measurements reveals the potential long-term stability of MOSFETs fabricated with these oxides. As in the case of silicon, improvement in the degree of the slow trapping instability in SiC MIS capacitors may be possible with further refinement of the insulator formation process.

3.3 Mobile Ionic Charge

Mobile ionic contamination in the oxides is another mechanism which results in shifts of the C-V curves with a voltage stress. Mobile ionic charge density can be determined from bias-temperature stress measurements [18]. Voltage stress experiments were performed on SiC capacitors with thermal oxide and CVD oxide insulating layers and on silicon MOS capacitors. The silicon MOS capacitors were fabricated using the same furnaces and procedures as the SiC devices for comparison purposes. Measurements on the silicon MOS capacitors showed a degree of mobile ionic charge comparable to that observed in the SiC thermal oxide capacitors. Since no other process in Si is known to resemble mobile ionic contamination, it is concluded that mobile ionic contamination is the cause of the similar instabilities observed in SiC and Si MOS capacitors fabricated for this study.

The effects of mobile ionic charge are only expected above room temperature. A positive voltage stress at elevated temperature (200 °C or more) results in a shift of the C-V curve towards negative voltages as ionic (positive) charges are repelled from the gate. At room temperature the same voltage stress results in no detectable shift of the C-V curve. The magnitude of the voltage shift is related to the mobile charge density, N_m, by:

$$N_m = \Delta V_{fb} * C_{ox}/qA. \qquad (5)$$

A sequential negative voltage stress at elevated temperatures results in a shift of the C-V curve back to its original position (towards more positive voltages) as ionic charges are attracted to the gate. The direction of a voltage-stress-induced shift in the C-V characteristics due to mobile ions is

opposite to that due to the slow trapping instability reported in the previous section.

C-V curves for a thermal oxide capacitor on SiC #975-5 before any stress, after a +7 V, 20-min stress at 300 °C, and after a sequential -2 V, 20-min stress at 300 °C are shown in figure 2. For this capacitor, a voltage stress of +7 V for 20 min at 300 °C results in a -1.2 V shift of the C-V curve. The entire shift is due to mobile ionic charges, corresponding to a density of 3.7 x 10^{11} cm^{-2}. A sequential positive voltage stress does not completely shift the C-V curve back to its initial position. Mobile charge densities for these SiC capacitors with thermal oxide insulators varied between about 1 and 4 x 10^{11} cm^{-2}. Some typical values of N_m are reported in table 1.

For these SiC capacitors, the shift due to mobile charges is partially obscured by the slow trapping mechanism that at room temperature results in a negative shift for a negative voltage stress. Thus there are two mechanisms which can shift the C-V curves of these SiC capacitors, and each can partially counteract the other. One mechanism is active at relatively high fields at room temperature and above (slow trapping); the other is active at lower fields but only at elevated temperatures (mobile ionic contamination).

The presence of mobile ionic charge is not endemic to SiC MIS capacitors, but is due to contaminants introduced during the capacitor fabrication process. As in the case of silicon technology, it is expected that careful process control could reduce the amount of mobile ionic charge to negligible levels (below 10^{10} cm^{-2}).

3.4 Effect of Temperature on MIS Capacitor Characteristics

Additional C-V measurements were taken as a function of temperature. C-V curves at approximately 25, 100, 200, and 300 °C were measured for selected thermal oxide capacitors. A series of C-V curves between room temperature and 250 °C for SiC #820-2 are shown in figure 3. These curves reveal a third mechanism that changes the shape of the SiC MIS capacitor C-V curves. As the measurement temperature is increased, greater numbers of interface traps become active, increasing the amount of stretchout in the C-V curves. As opposed to the shifts induced by a voltage stress, this change in stretchout is not permanent, but is solely dependent on the measurement temperature. After taking C-V curve 4 of figure 3 at 260 °C, the initial C-V curve is again measured at room temperature.

While taking C-V data at elevated temperatures, the application of negative voltages can result in significant negative shifts of the C-V characteristics due to slow trapping effects. Even briefly applying a field of 1.5 x 10^6 V/cm at 300 °C can result in a shift of several volts. Thus the voltage range of C-V curves reported in figure 3 is limited to less than the threshold for significant slow trapping to occur.

These measurements allowed the change in C-V response with temperature due to additional interface traps active at that temperature to be separated from changes due to charge trapping and mobile ion drift during the voltage sweep.

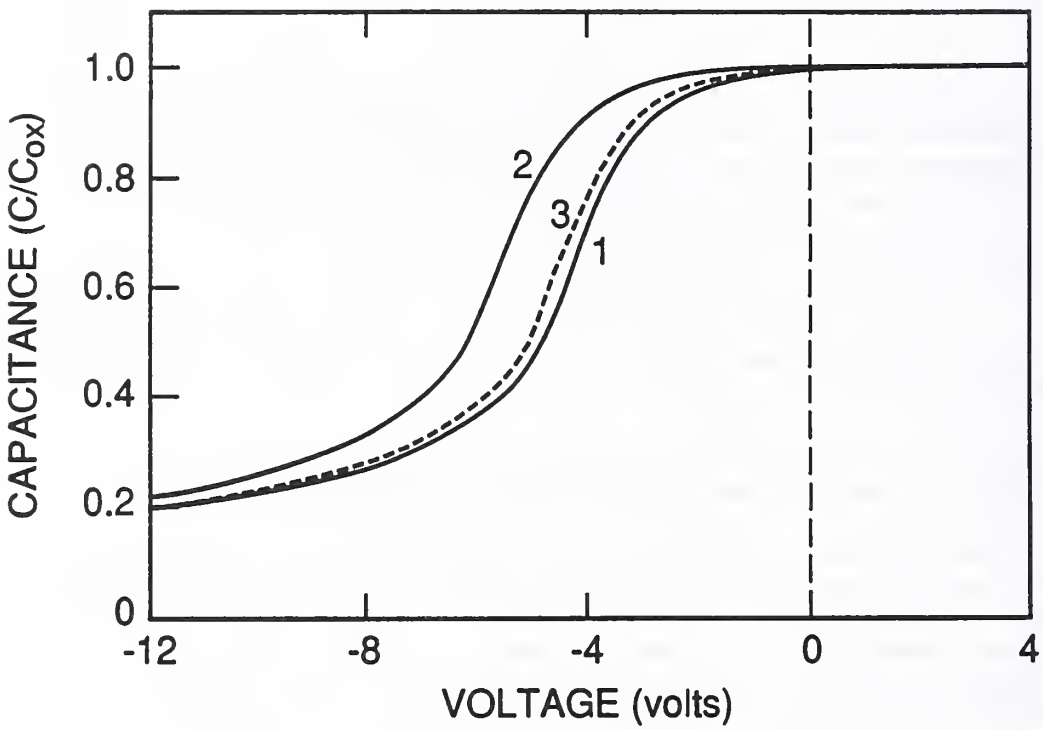

Figure 2. C-V curves of SiC MIS capacitor (SiC #975-5) after a bias-temperature stress showing the effect of mobile ionic charge. 1) Before any voltage stress; 2) after +7 V, 20-min, 300 °C stress; 3) after -2 V, 20-min 300 °C sequential stress. The mobile charge density, N_m, for this device was determined from this bias-temperature cycle to be 3.7 x 10^{11} cm^{-2}.

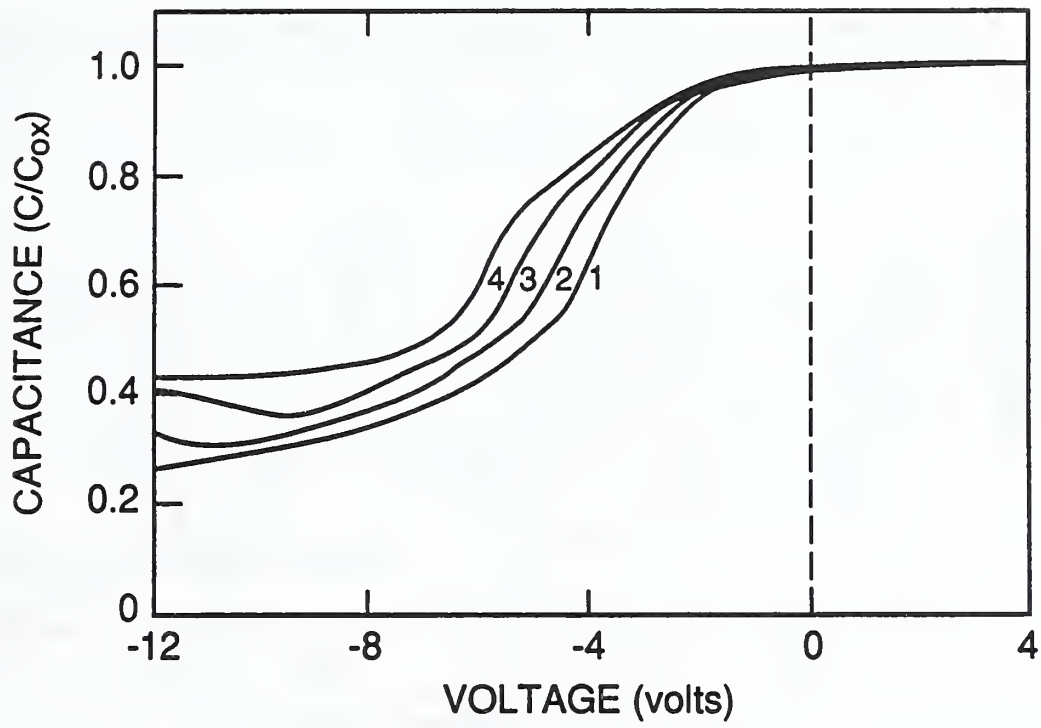

Figure 3. C-V characteristic of a SiC MIS capacitor (SiC #820-2) at 1) room temperature, 23 °C; 2) 115 °C; 3) 175 °C; and 4) 260 °C. The voltage range is limited so that little slow trapping or mobile ion drift should occur.

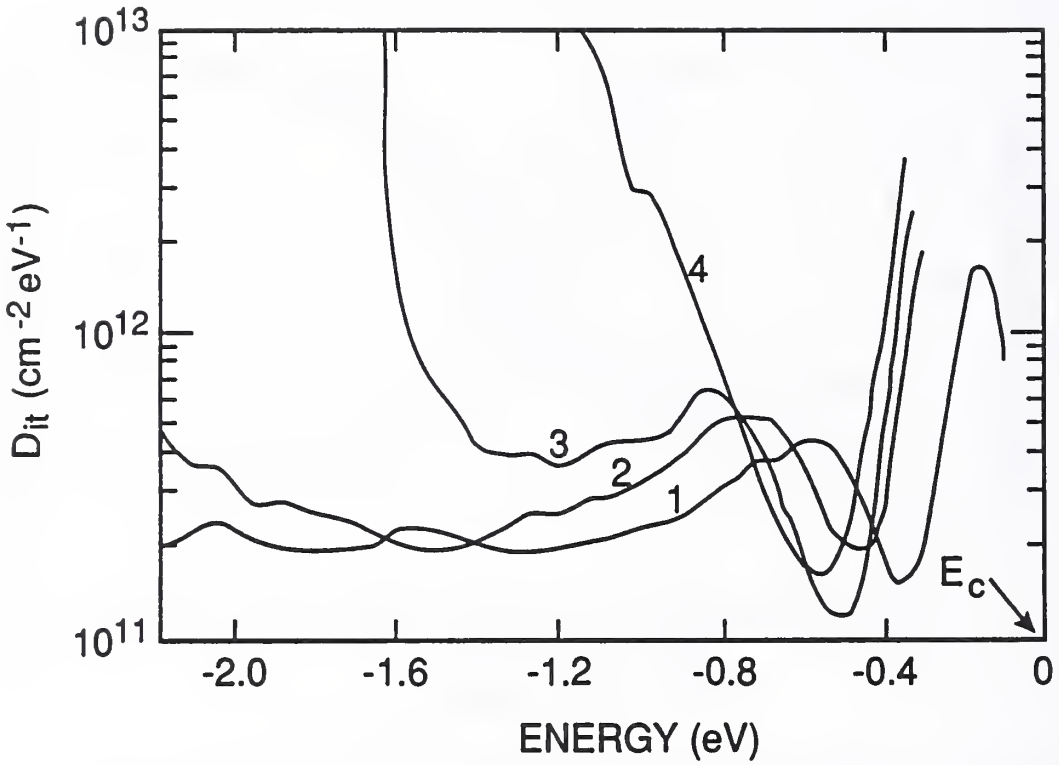

Figure 4. D_{it} vs. temperature from C-V curves in figure 3 at 1) room temperature, 23 °C; 2) 115 °C; 3) 175 °C; and 4) 260 °C. The D_{it} profile is referenced with respect to conduction band edge at each temperature.

From inspection of the C-V curves, it is seen that increasing temperature decreases the extent that the capacitors enter deep depletion. The apparent minimum (inversion) capacitance increases with temperature, indicating that the substrate is behaving more highly n-type. The distortion in shape from a theoretical curve increases with temperature. The 260 °C C-V curve in figure 3 has a very distinct bulge from the expected behavior without interface traps.

Interface trap profiles determined via the Terman method [16] for the C-V curves in figure 3 are shown in figure 4. Increasing temperature decreases the bandgap slightly. Mid-gap is ψ_b from flatband ($\psi_S = 0$), while ψ_b decreases with temperature. The D_{it} profiles shown in figure 4 are referenced with respect to conduction band edge at each temperature.

As care has been taken to reduce any effects due to slow trapping, the changes in the C-V curves are expected to be mostly due to changes in the number of active interface traps. The peak in D_{it} is shifted away from the conduction band edge towards mid-gap with increasing temperature. The peak height increases with temperature. At 260 °C, the D_{it} profile has evolved into a large broad peak that fills the lower portion of the bandgap.

In summary, a series of voltage stress measurements on SiC MIS capacitors has been completed. These measurements complete the determination of all oxide charge components present in SiC capacitors: fixed charge, interface trap charge, bulk oxide charge, and mobile ionic charge. A mechanism whereby bulk oxide and interface trap charges are charged/created by large electric fields has been identified and quantified. The complete determination of the charge components present in SiC MIS capacitors is important in determining the eventual operating properties of MOSFETs fabricated with SiC.

4. CURRENT-VOLTAGE MEASUREMENTS

4.1 Current-Voltage Characteristics

Current-voltage (I-V) measurements were made on selected SiC capacitors with thermal oxide or CVD oxide insulators. These measurements were made with a Hewlett-Packard 4140B Pico-Amp Meter. From current-voltage measurements, the insulator resistivity and breakdown fields can be precisely determined. Information about the charge conduction mechanism in the insulating layer can also be deduced from the I-V behavior [33-34].

A typical I-V measurement of a SiC MIS capacitor is shown in figure 5. In the positive voltage direction (towards accumulation), three regions are seen. At low voltages only extremely low currents flow. At higher voltages, rapidly increasing currents are seen. At some high voltage, breakdown occurs and the current suddenly increases to the limit of the meter. In the negative voltage direction (towards inversion), the same three regions are seen. At large negative voltages, corresponding to voltages where the C-V curve recovers from deep depletion, the current is seen to decrease with increasing voltage for part of the I-V characteristics. This dip in the I-V characteristics is related to the bulk oxide traps and is discussed later.

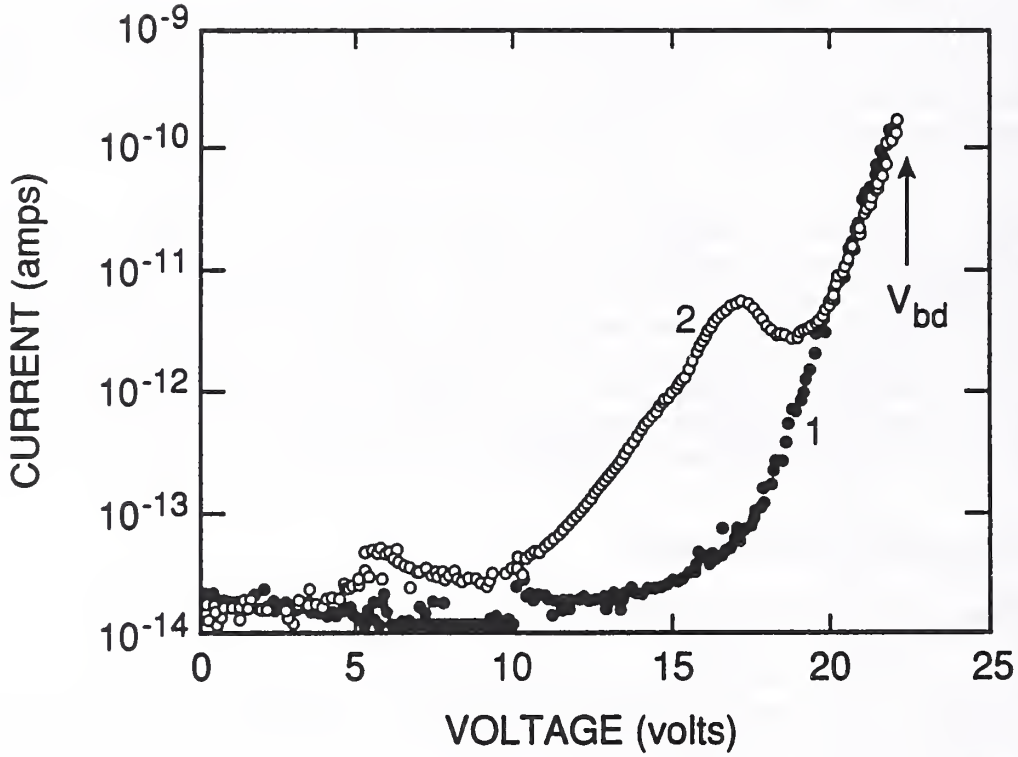

Figure 5. Typical I-V characteristics for a SiC MIS capacitor (#820-2) in the 1) forward (accumulation) and 2) reverse (depletion) directions.

4.2 Insulator Breakdown Field and Resistivity

Detailed I-V measurements allowed a precise determination of the oxide resistivity and the capacitor breakdown voltage. The resistivity was estimated in the approximately linear I-V region seen at the lowest voltages. It was assumed that the low currents seen at these voltages were due to ohmic conduction in the oxide. The equivalent ohmic resistivity of the oxide was thus estimated as:

$$\rho = (V/T_{ox})/(I/A) \tag{6}$$

where V is the applied voltage, T_{ox} is the oxide thickness, I the measured current, and A the capacitor area.

An accurate determination of oxide resistivity was difficult because of the extremely small currents (about 0.1 pA or less at 10 V bias). For resistivities greater than about 5×10^{16} Ω-cm, eq (6) could not be applied because the current was too small to be resolved. There was a large amount of variation in ρ from device to device. The average resistivity of the thermal oxide layer on SiC was about 10^{16} Ω-cm, and some capacitors had greater resistivities.

The breakdown fields were easy to determine from I-V characteristics as a very sharp increase in current of six or more orders of magnitude occurred. This was a destructive measurement: devices no longer displayed a C-V characteristic after breakdown was exceeded. When measured in the accumulation region, the breakdown field is simply:

$$E_{bd}=V_{bd}/T_i \tag{7}$$

where V_{bd} is the voltage at which breakdown occurred and T_i is the insulator thickness. Breakdown fields for thermal oxides on as-grown SiC had a narrow range between 3.1 and 3.8×10^6 V/cm. The average breakdown field was 3.3×10^6 V/cm. Breakdown fields of the silicon MOS capacitors fabricated for comparison purposes were 8 to 10×10^6 V/cm. Typical values of E_{bd} are reported in table 2.

The difference in E_{bd} between MOS capacitors on Si and SiC can be attributed to the rough surface of the as-grown SiC. A smooth SiC surface was produced by mechanical polishing with 1-μm diamond paste. This crystal was then oxidized, and the oxide etched off to remove any surface damage.* MOS capacitors were fabricated on this polished SiC using a wet thermal oxide grown at 1050 °C for 6 hours. Oxide thickness was approximately 560 Å. E_{bd} for capacitors on this crystal were 7 to 8×10^6 V/cm.

---

* SiC grown and polished at North Carolina State University in 1986.

TABLE 2 TYPICAL MEASURED BREAKDOWN FIELDS OF INSULATING LAYERS IN SiC MIS CAPACITORS

SiC ID#	Insulator	T_{ox} (Å)	E_{bd} (x 10^6 V/cm)
820-2*	1150 °C thermal	655	3.3
975-5	1050 °C thermal	672	3.3
975-6*	1100 °C thermal	593	3.4
975-8	1150 °C thermal	600	3.3
975-9*	1200 °C thermal	589	3.6
916-9*	CVD, densified at 1000 °C	595	3.2
Average			3.3
Polished SiC	1050 °C thermal	558	7-8
Typical silicon			8-10

* SiC grown on (001) silicon; others were grown on slightly off-axis Si.

Table 2 Typical results of current-voltage measurements. Values presented are averages from measurements on five or more capacitors for each sample. Oxide thickness is calculated by fitting the observed I-V characteristic to the Fowler-Nordheim equation.

4.3 Fowler-Nordheim Tunneling and Determination of the SiC-SiO_2 Barrier Height

Information about the charge conduction and trapping mechanisms in the insulating layer can be deduced from the I-V behavior [33-34].

Electronic conduction in silicon MOS capacitors is known to be limited by Fowler-Nordheim emission [19, 35-36]. Fowler-Nordheim emission is the tunneling of electrons from the vicinity of the electrode Fermi level through the forbidden energy gap into the conduction band of the oxide. F-N conduction is identified by a J/F^2 dependence of the form [19]:

$$J/F^2 = Ce^{-\beta/F} \tag{8}$$

where J is the current density through the insulator and F is the electric field applied to the insulator. The pre-exponential term, C, and β [19] are dependent on the effective mass, m_{ox}, of an electron in the insulator, and ϕ_B, the barrier between the emitting electrode and the insulator. A plot of $\log(J/F^2)$ vs. $1/F$ of a capacitor limited by F-N emission will be a straight line with slope β and intercept C from which m_{ox} and ϕ_B can be determined.

I-V measurements were made on some MOS capacitors on silicon to verify the software and interpretations of data. Figure 6 shows the I-V characteristics of a silicon MOS capacitor. The theoretical behavior (solid line) is calculated using the accepted values of the Si-SiO_2 barrier height for electrons of 2.9 eV [37] and an electron effective mass in the oxide of $0.5*m_e$, where m_e is the electron mass in free space [35]. The oxide thickness estimated from the slope of the F-N current [19] for this device was approximately 890 Å. This is in agreement with the thickness determined from the oxide capacitance and reflectance spectrometry measurements. The plot of $\log(J/F^2)$ vs. $1/F$ is shown in figure 7 and displays linear behavior over four orders of magnitude.

All SiC samples with thermal oxides displayed the expected Fowler-Nordheim I-V characteristics when a positive voltage was applied. Positive voltages imply that electrons are tunneling from the substrate into the oxide. I-V characteristics from a capacitor on as-grown SiC (#975-6) and from a capacitor on polished SiC are shown in figure 8. A very low leakage current is seen before significant tunneling current is observed. Compared to silicon MOS capacitors, appreciably greater F-N currents flow at the same voltages for the as-grown SiC material. A F-N plot showing the expected linear behavior for both SiC MOS capacitors in figure 8 are shown in figure 9.

The SiC-SiO_2 barrier height was determined from the slope and intercept of the F-N plots of the I-V characteristics [19]. It was assumed that the electron effective mass in SiO_2 ($0.5\ m_e$) would be the same for oxides on silicon and SiC. The oxide thickness on SiC was estimated from the oxide capacitance in strong accumulation. Oxide thickness determined in this manner is relatively inaccurate and is a source of error in the determined barrier height.

Measurements were made on five capacitors on five different as-grown SiC samples. The apparent barrier height on these devices was determined to be

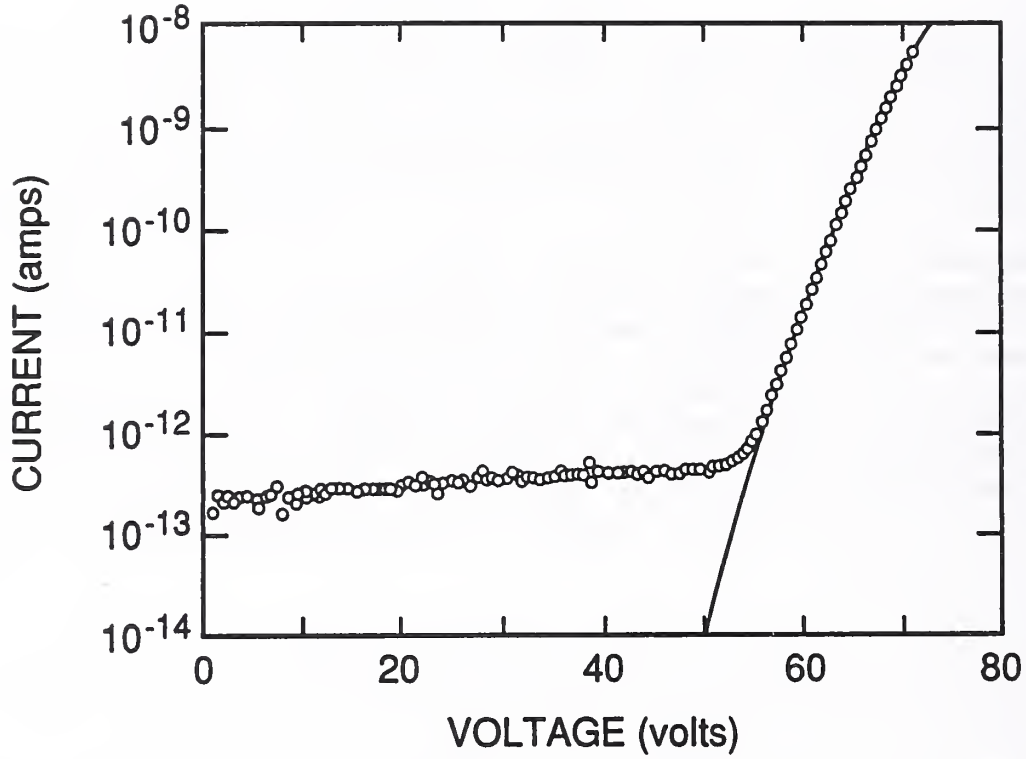

Figure 6. Measured current-voltage characteristics (points) of a silicon MOS capacitor. The theoretical Fowler-Nordheim tunneling current (solid line) is calculated using the known Si-SiO_2 barrier height of 2.9 eV. The oxide thickness of 890 Å was determined from the I-V using the method in [36].

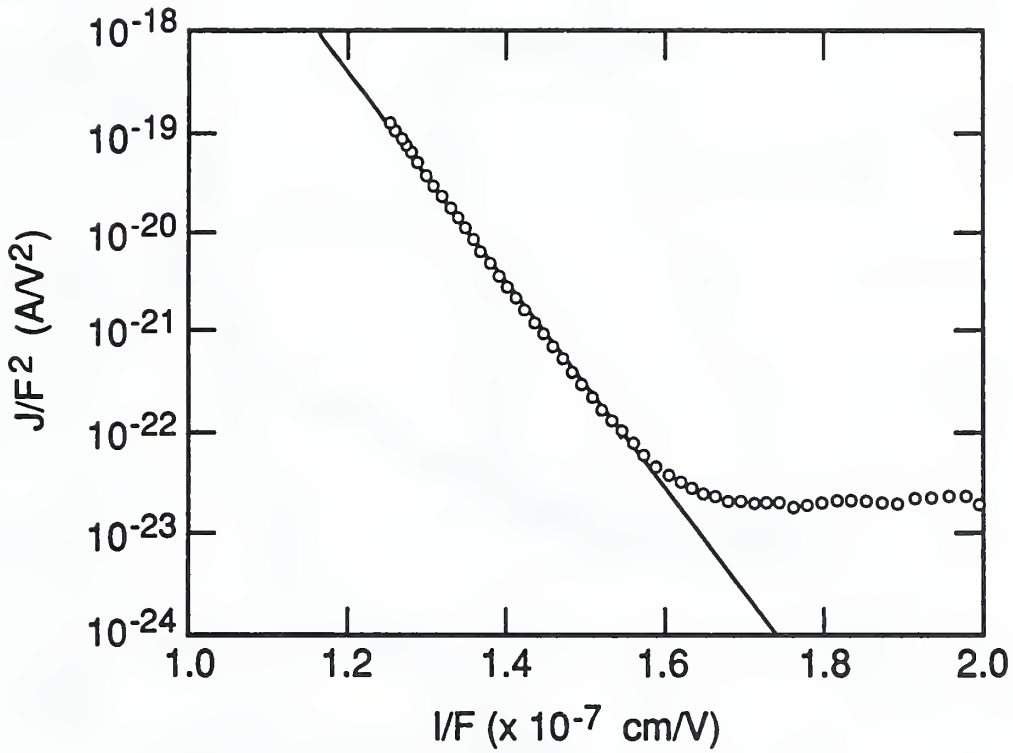

Figure 7. Fowler-Nordheim plot of I-V data in figure 6 showing the linear relation between J/F^2 (plotted on the vertical axis) and 1/F (plotted on the horizonal axis).

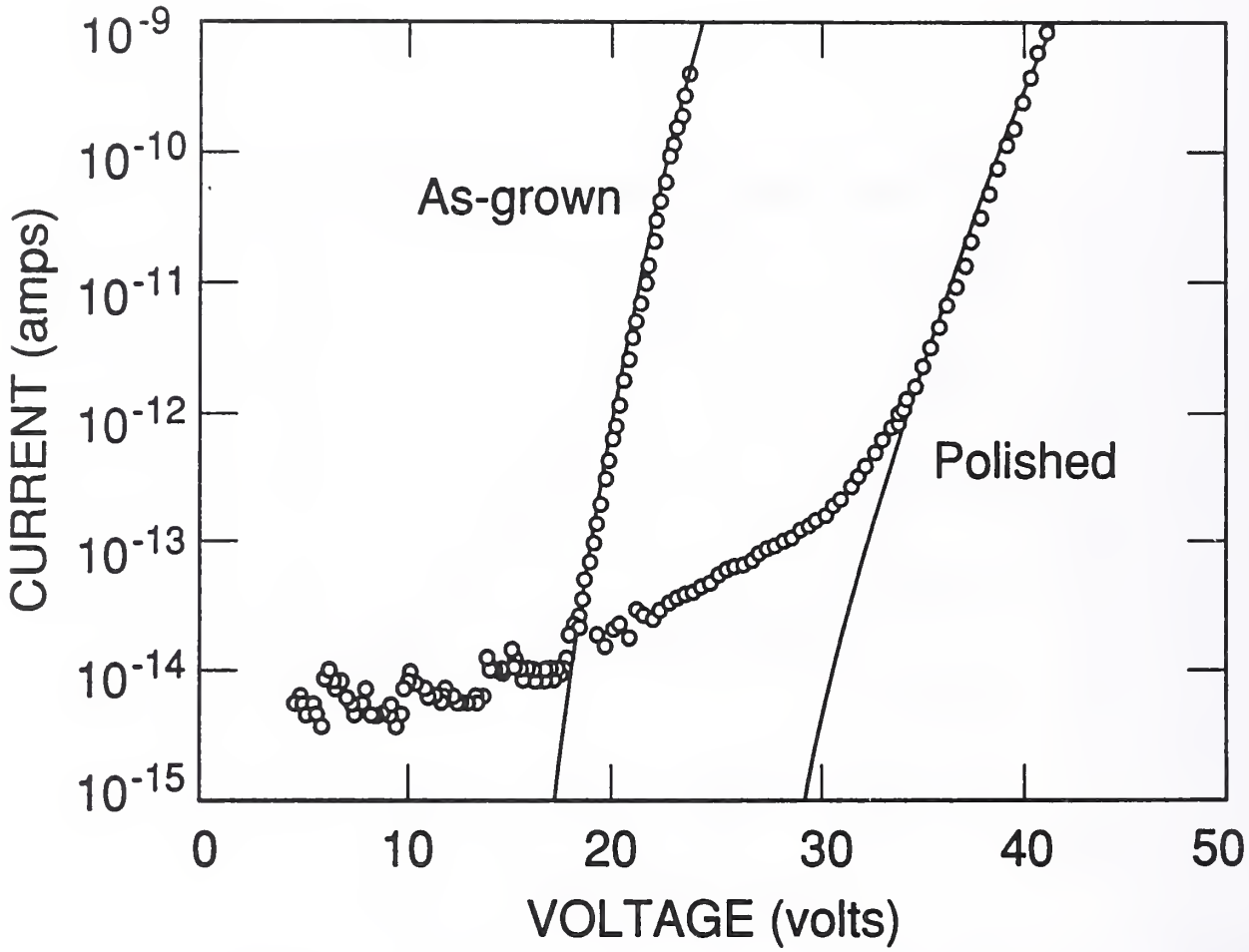

Figure 8. Current-voltage characteristic of an MOS capacitor on 1) as-grown SiC (SiC #975-6) and 2) mechanically polished SiC (from NCSU). The oxide thickness was determined from the oxide capacitance in accumulation. The theoretical (solid) curve is calculated for curve 1) from t_{ox} = 664 Å, ϕ_B = 1.76 eV and m_{ox} = 0.5*m_e and for curve 2) from t_{ox} = 558 Å, ϕ_B = 2.90 eV and m_{ox} = 0.5*m_e.

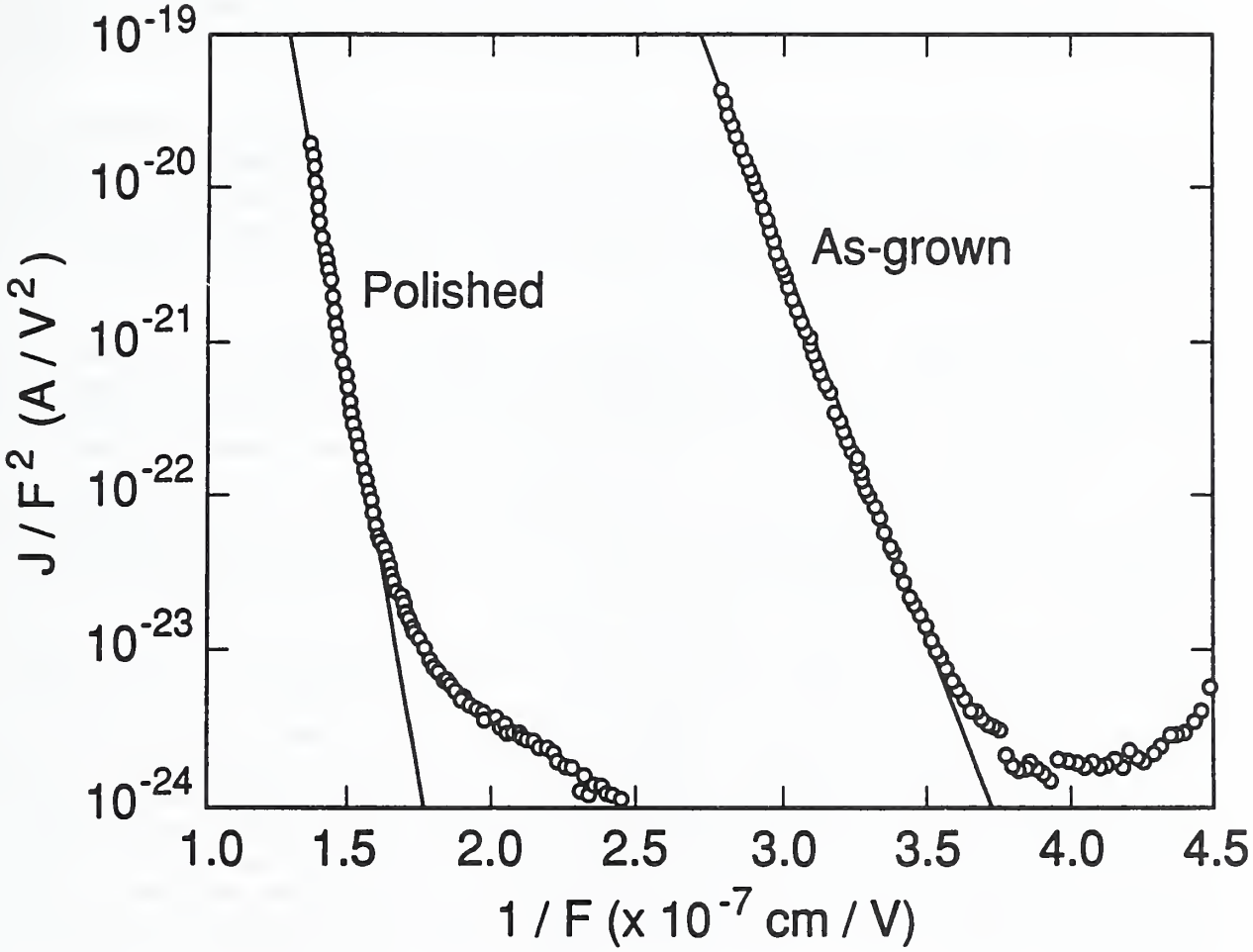

Figure 9. Fowler-Nordheim plot of SiC MIS capacitor I-V data from figure 8; 1) as-grown SiC, and 2) polished SiC.

1.8 ± 0.1 eV. The rough surface of the as-grown SiC layers results in thin spots in the oxide or regions of enhanced electric field near sharp protrusions [38]. Either non-ideality would result in current flowing at lower fields and an apparently lower SiC-SiO_2 barrier height.

Significantly greater electric fields were required to achieve the same current density for MOS capacitors on the polished SiC, compared to the as-grown material. From I-V measurements, a barrier height for electrons tunneling from cubic SiC into SiO_2 as large as 2.9 eV was measured for capacitors on the polished SiC. The actual SiC-SiO_2 barrier height is calculated to be about 3.1 eV, using an electron affinity of cubic SiC of χ = 4.3 eV [39], an electron affinity of SiO_2 of 0.95 eV, and assuming barrier height lowering comparable to that of the Si-SiO_2 interface.

The barrier height determined from I-V measurements of capacitors on the polished SiC varied from about 2.6 to 2.9 eV. While the surface of the SiC appears nearly featureless (even under 70X magnification) some microscopic roughness may remain. Thus, the value of 2.9 eV should be regarded as a lower limit of the actual barrier height that would be measured with an ideal, atomically abrupt SiC-SiO_2 interface.

For negative voltages, there is a dip in the current, roughly correlated with the recovery of the capacitance from deep depletion. Negative voltages imply that electrons are tunneling from the gate and that holes could be injected or tunneling from the substrate. Similar ledges or dips have been reported in the I-V characteristics of silicon MOS capacitors when the current reaches a level at which SiO_2 traps start to fill significantly [40]. The charged traps build up an internal electric field opposed to the increasing applied field. The field is held approximately constant until the traps are filled which keeps the current through the device constant.

For silicon under high negative fields, it has been suggested [41] that hot holes are generated by impact ionization by electrons entering the silicon from the oxide conduction band. These hot holes could then tunnel from the SiC valence band into the oxide where they become trapped. This phenomenon is an attractive explanation as it accounts for both the generation of an inversion layer in the SiC through a process that creates holes in the SiC substrate and the positive charge creation in the oxide as reported in section 2.2. Electron-hole pairs may also be created within the oxide via impact ionization by electrons injected into the SiO_2 by Fowler-Nordheim tunneling.

In summary, a series of current-voltage measurements have been completed on silicon and SiC MOS capacitors. For MOS capacitors on SiC, Fowler-Nordheim tunneling was identified as the conduction mechanism and a SiC-SiO_2 barrier height of 2.9 eV was determined. The surface roughness of the as-grown SiC lowers both the electric breakdown field and the apparent barrier height. For optimal performance of MOSFETs fabricated with these materials, the surfaces may need to be polished.

5. DEEP-LEVEL TRANSIENT SPECTROSCOPY

Deep-level transient spectroscopy (DLTS) is a technique to detect, identify, and characterize deep traps in semiconductors. The DLTS technique is based on the measurement of the transient capacitance resulting from the deep levels in the depletion region of a diode. The transient is normally excited by repetitive pulsing of the diode from a forward (or zero bias) to a reverse bias. During the forward-bias pulse, the deep levels fill with electrons (or holes for p-type material). Following the re-establishment of the reverse bias, the electrons are thermally emitted from the levels with an emission rate which depends strongly on temperature. This gives a change in capacitance which, in the ideal case, decays exponentially to the equilibrium value.

The data acquisition parameters are the pulse voltage, V_{pul} between the reverse- and forward-bias voltages, V_r and V_f; the pulse duration, τ_{pul}; the fill time (time at forward-bias), t_{fill}; and the delay times t_1 and t_2 after the voltage pulse at which the capacitance is measured. The DLTS signal is the transient capacitance $\Delta C = C(t_1) - C(t_2)$. For the system used in this work, ΔC is measured with a boxcar averager. The transient capacitance is plotted as a function of temperature. A peak in the DLTS signal is seen when the rate window or time constant of the boxcar averager matches the emission time constant of a trap. Analysis of the transient can give the trap concentration, emission time constant, capture cross section, and activation energy for thermal emission [42].

The DLTS technique works best with pn-junction or Schottky barrier diodes. There are some reports of using DLTS with MOS capacitors [43-45], primarily to measure interface trap properties. It may be possible to determine some information about deep levels in the semiconductor from DLTS measurements on MOS capacitors [43]. DLTS measurements have been reported for pn-junction diodes in SiC [46] and Au to SiC Schottky diodes [47]. No previous reports have been made of DLTS for MOS capacitors on SiC.

The use of an MOS capacitor for DLTS measurements introduces several complicating considerations. The type of DLTS response from an MOS capacitor is strongly dependent on the magnitude of the reverse bias [44]. The effect of surface states on the DLTS signal can be isolated from the effect of bulk traps by using a small reverse bias so that all the surface states are depleted, while most of the bulk traps remain populated. A larger reverse bias will form a depletion region, and in this case, both surface states and the bulk traps in the depletion region will contribute to the DLTS signal. A reverse bias large enough that the inversion point is reached will result in a large, spurious transient due to the capacitor recovery from deep depletion to inversion. Any measurement with which a signal from deep levels in the bulk can be detected will also include signal from surface states.

As an alternative to using MOS capacitors for DLTS measurements, Au-on-SiC Schottky diodes were fabricated. After a cleaning procedure [47], 5000 Å of Au was sputter deposited onto a SiC layer. Contact dots of 50, 75, and 250 μm were patterned onto the SiC. These Au-to-SiC dots formed rectifying Schottky

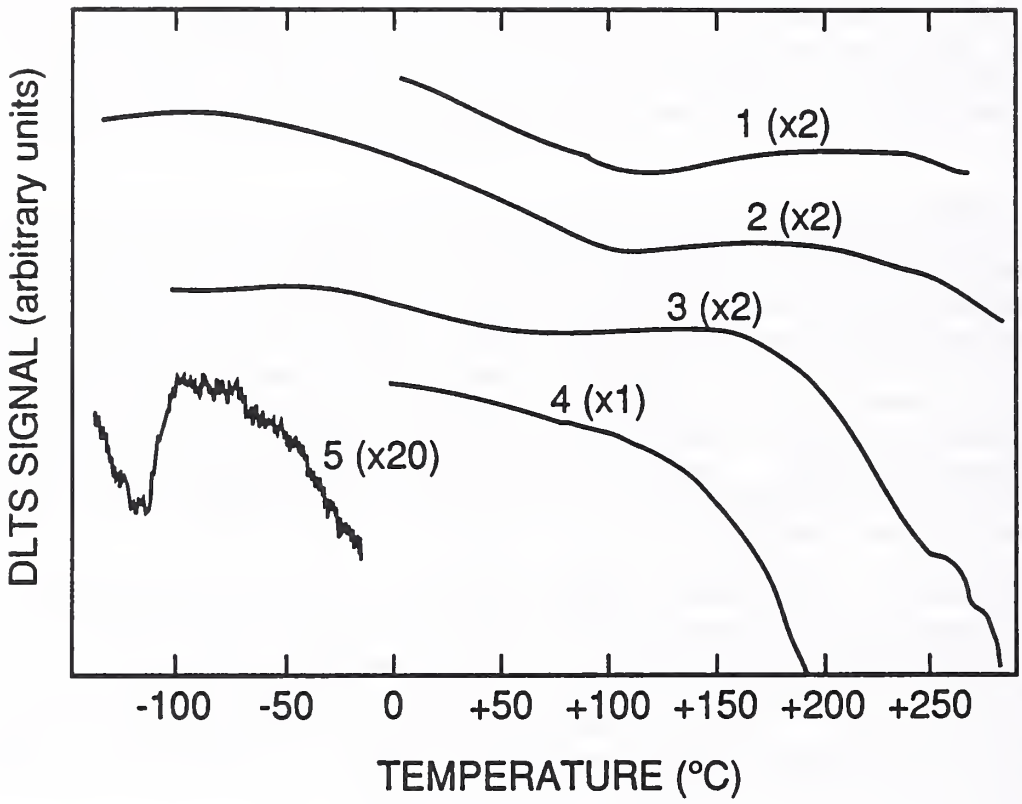

Figure 10. DLTS traces for a SiC MIS capacitor with thermal oxide insulator (SiC #820-2) showing the change in shape of the response for four different bias sequences. Traces have been displaced vertically for clarity. Curves 1, 2, and 3 are multiplied x2 relative to curve 4.

Curve 1 -- Pulse into depletion with V_r: -6 V, V_f: 0 V, t_{fill}: 4 mS, t_1: 4.0 mS, t_2: 19.8 mS. Curve 2 -- Pulse into depletion with V_r: -7 V, V_f: +3 V, t_{fill}: 2 mS, t_1: 2.5 mS, t_2: 19.9 mS. Curve 3 -- Pulse into deep depletion with V_r: -10 V, V_f: -5 V, t_{fill}: 2 mS, t_1: 3.7 mS, t_2: 48.6 mS. Curve 4 -- Pulse into inversion with V_r -15 V, V_f: 0 V, t_{fill}: 2 mS, t_1: 3.1 mS, t_2: 17.7 mS. Curve 5 -- Low-temperature portion of curve 4, multiplied x20.

diodes. However, the Au had very poor adhesion to the SiC, and the diodes were not sufficiently stable with time to successfully make DLTS measurements.

Typical DLTS traces obtained for a SiC MIS capacitor with a thermal oxide insulating layer (SiC #820-2) are shown as figure 10. Data acquisition conditions are listed in the figure caption. Peaks in DLTS signal appear as valleys in figure 10. Three observations about the DLTS response of SiC MOS capacitors were made:

1) The transient due to inversion layer generation was seen. It is visible as the large increase in DLTS signal at high temperatures in curves 1 to 4. These four curves used progressively larger reverse bias voltages, resulting in wider depletion regions. This transient increased steadily with increasing reverse-bias voltage. With a reverse bias of -15 V (curve 4), this transient dominates the response, and no other features are discernible in the response.

2) For curves 1, 2, and 3, a broad, shallow peak, partially obscured by the large signal due to inversion charge generation, was seen at about +100 °C. As this peak is seen for all reverse-bias voltages investigated, it may be due to the interface states.

3) At very low temperatures, a small peak, shown as curve 5 of figure 10, was occasionally observed. The peak magnitude, in most cases, was about that of the noise in the DLTS signal. It could not be reliably determined if this peak was due to a deep-level or a measurement artifact. If it is due to a trap in the bulk, it would be a very shallow (close to the conduction band) level.

In conclusion, a brief survey of DLTS measurements on SiC MIS capacitors did not yield any large or obvious peaks that could be attributed to bulk deep levels. Interpretation of the DLTS signal would be greatly simplified if pn-junction or Schottky barrier diodes were available. It was possible to measure the capacitance transient as a function of temperature of the SiC MIS capacitors after they were pulsed into depletion. This implies that the Zerbst's analysis [48], which yields minority carrier lifetimes and deep-level detection, could be performed with these devices.

6. CONCLUSIONS (Electrical Characteristics of SiC MIS Capacitors)

A wide variety of fabrication processes and electrical characterization techniques for SiC MIS capacitors have been examined. Many of the electrical characterization techniques commonly applied to silicon MOS capacitors have now been applied to SiC MIS capacitors. From this comprehensive study, the following picture of the MIS capacitors on SiC has emerged:

Capacitance and Conductance vs. Voltage Behavior: Similar to silicon and contrary to GaAs, the native oxide at the cubic SiC interface is unpinned. The capacitance of MIS structures shows accumulation, depletion, and inversion regions. SiC resembles silicon at low temperature due to its large bandgap. A consequence of the large bandgap is an extremely low generation/ recombination rate for minority carriers at room temperature. As discussed in

the previous report [15], the SiC MIS capacitor C-V curves show three distinct features which are related to the large bandgap: 1) deep depletion, 2) recovery from deep depletion, and 3) a stagnant inversion layer. At 300 °C, SiC MIS capacitors resemble silicon MIS capacitors at room temperature.

Similar to silicon MOS capacitors, the conductance of SiC MIS capacitors shows a large peak with voltage due to the response of interface traps. The interface trap level density determined from the Terman method and from the peak of the G-V response are in fair agreement.

Oxide Charges: Any discussion of oxide charges must be qualified by the fact that these parameters are highly process- and material-dependent. Considerable variation was seen from SiC to SiC sample and even from device to device on the same SiC crystal. In general and in view of the rapid progress being made in SiC crystal growth, any number reported for an oxide charge of a specific SiC capacitor should be regarded as an upper limit of what may ultimately be achieved.

In any comparison of the oxide charges of a cubic SiC MOS capacitor with a silicon capacitor, it should be remembered that the lattice constant of SiC is 4.36 Å, while that of silicon is 5.43 Å. This means that SiC has about 1.5 times more surface atoms than a comparable orientation of silicon. It is well known that the density of charges measured for a silicon MOS capacitor is highly orientation dependent and is directly proportional to the number of surface atoms. Thus, it would be expected that cubic SiC will have oxide charges at least 1.5 times larger than silicon.

1. *Fixed Oxide Charge Density* (N_f) -- Fixed oxide charge was determined from the amount of shift of the measured C-V curve from the ideal at the flatband voltage. N_f observed in this study was 4 to 9 x 10^{11} cm^{-2}.

2. *Interface Trap Level Density* (D_{it}) -- Interface trap level density was determined from the high-frequency C-V curve using the Terman method. At mid-gap this was in the range 0.5 to 2 x 10^{11} cm^{-2} eV^{-1}. A peak 2 to 10 times the mid-gap value was seen about 0.6 eV below the conduction band edge. Determination of D_{it} from G-V measurements confirms the order of magnitude of D_{it} determined from the Terman method.

3. *Bulk Oxide Trapped Charge* (N_{ot}) -- The change in oxide trapped charge produced by a voltage stress was determined using the method of Winokur et al. [17]. The sense of the voltage shift indicates that positive charge has been created in the oxide. N_{ot} is increased by up to 5 x 10^{11} cm^{-2}. It cannot be ascertained if these traps were initially present and were charged by the stress, or if they were created and charged by the stress.

4. *Mobile Ionic Charge* (N_m) -- The mobile ionic charge was determined from the effects of voltage stress at elevated temperature. Ionic contamination is introduced into the devices during processing, and it should be possible to completely eliminate it. Regardless, the lowest N_m seen for any SiC capacitor in this study was about 5 x 10^{10} cm^{-2}.

Stability: Three mechanisms were seen that affected the long-term stability of these SiC MIS capacitors. They were most exaggerated when the devices were subject to extreme operating conditions (high electric field or high temperatures).

1. *Negative Bias Temperature Instability (Slow Trapping)* -- At room temperature, a negative stress field (above a threshold field of about -1.5×10^6 V/cm) results in a shift of the C-V characteristics in the negative direction. The direction of the shift indicates that positive charge has been created in the oxide. A positive stress does not result in a corresponding shift. This is similar to the slow trapping instability in silicon MOS capacitors. Analysis of the C-V curve indicates that oxide traps, N_{ot}, of up to 5×10^{11} cm^{-2} have been charged or created by the stress field. D_{it} has also been increased.

2. *Positive Bias Temperature Instability (Mobile Ionic Contamination)* -- At elevated temperatures (100 to 300 °C), a positive stress field results in a shift of the C-V characteristics in the negative direction. A sequential negative stress shifts the C-V curve back in the positive direction to its original position. This type of instability is due to mobile ionic charge. This instability is not endemic to SiC MIS capacitors, but is due to contamination during processing or afterwards.

3. *D_{it} increases with temperature* -- By minimizing the effects of both slow trapping and mobile ion drift, it was found that the temperature increases the number of interface traps that respond at a given gate voltage. At 300 °C, a large density of traps deep in the bandgap (far from the conduction band) are active. This is solely related to the temperature; room-temperature characteristics return when the device is cooled.

Current vs. Voltage Behavior: From I-V measurements, thermal oxides on SiC in this study were found to typically have resistivities of about 10^{16} Ω-cm and breakdown electric fields of 3.3×10^6 V/cm. Both of these values are less than expected for SiO_2 on silicon. MOS capacitors on polished cubic SiC had E_{bd}'s of 7 to 8 $\times 10^6$ V/cm, indicating that the low E_{bd} of the as-grown SiC is due to surface roughness.

In the depletion region, the I-V characteristics were found to have a dip in current at voltages corresponding roughly to the recovery of the capacitance from deep depletion. The dip in current is related to the slow trapping shifts of the C-V curves. No slow trapping is seen at low fields corresponding to low oxide currents. As the field increases, a progressively larger electron current (probably from tunneling from the gate into the oxide) is seen in the capacitors. It may be that some electrons are injected from the oxide into the SiC, creating electron-hole pairs in the SiC by impact ionization. Some holes tunnel into the oxide where they become trapped, leading to the observed shifts in the C-V curves (slow trapping) and the dip in the current. The hole recombination rate in SiC is expected to be low due to the large bandgap.

In the accumulation region, the I-V characteristics were found to follow the

classic Fowler-Nordheim relation. Fitting the measured I-V data to the F-N relation, a value for the SiC-SiO_2 barrier height for electron tunneling, ϕ_B, of 2.9 eV with $m_{ox} = 0.5*m_e$ was determined for a polished SiC surface. The apparent barrier height measured for as-grown SiC to SiO_2 was 1.8 eV. Much larger current densities at the same electric field were seen for MOS capacitors on as-grown SiC compared to the polished SiC.

Prospects for High-Temperature SiC MOSFETs: Operation of MOSFETs in cubic SiC with thermal oxide dielectrics has been reported at temperatures as high as 650 °C [7]. Silicon transistors would not function at all at these temperatures; the junctions would no longer rectify. SiC MOSFETs still operate, but no mention is made of their long-term stability at such elevated temperatures. The metal-semiconductor contacts and the gate insulator may well prove the part of the device that will fail first at high temperatures. For this reason, the long-term stability of an MIS capacitor on SiC at high temperature is of concern.

The persistence of high levels of traps in SiC MIS capacitors, even after considerable process optimization, indicates that there may be factors intrinsic to SiC that lead to traps. Factors that may serve to increase the trap density in SiC MIS capacitors include: the rough as-grown surface of SiC, defects in the SiC, residual carbon in thermal oxides, and the stress in the SiC from being an epitaxial layer on silicon. The rough as-grown surfaces of the SiC used in this study were seen to lower E_{bd} and to increase the current density of MIS capacitors.

We have made considerable progress in understanding how an MIS capacitor on a wide bandgap semiconductor functions. Of particular interest to future investigators should be the trapping properties and stability at high temperature. SiC-based devices have the potential to operate at temperatures higher than any common previous semiconductor devices. Thus, the behavior of device components (such as MIS capacitors) at these high temperatures and their long-term stability and reliability will be an important field for future study.

The SiC MIS capacitors with thermal oxide insulating layers fabricated for this study continued to be operational (though somewhat altered) even after stress fields in excess of the normal operation point at 300 °C. The devices displayed adequate stability and durability to be considered for the gate insulators of MISFETs operating at high temperatures.

Acknowledgments

The author thanks Dr. D. B. Novotny and the NIST Semiconductor Processing Research Laboratory staff for the fabrication of the SiC MIS capacitors used for this work. Dr. J. R. Lowney provided many useful discussions on the interpretation of the voltage stress and current-voltage measurements. Dr. R. E. Avila of the University of Puerto Rico provided helpful input on the extraction of interface trap level density from the peak of the conductance vs. voltage characteristics. Mr. W. R. Thurber assisted greatly with the DLTS measurements.

References

1. S. Nishino, J. A. Powell, and H. A. Will, Production of Large-Area Single-Crystal Wafers of Cubic SiC for Semiconductor Devices, Appl. Phys. Lett. 42, 460-462 (1983).

2. L. A. Tang, J. A. Edmond, and J. W. Palmour, Discrete Devices in 6H-Silicon Carbide, Extended Abstracts of the 176th Electrochemical Society Meeting, Hollywood, Fla, 1989, p. 705.

3. J. A. Powell, J. B. Petit, L. G. Matus, and S. E. Lempner, Growth and Characterization of 3C-SiC and 6H-SiC Grown on 6H-SiC, to be published in The Proceedings of the 3rd International Conference on Amorphous and Crystalline SiC, Howard University, Washington D.C., April 1990.

4. Y. Kondo, T. Takahashi, Y. Hayashi, E. Sakuma, S. Misawa, H. Daimon, M. Yamanaka, and S. Yoshida, Experimental 3C-SiC MOSFET, IEEE Electron Dev. Let. EDL-7, 404-406 (1986).

5. K. Shibahara, T. Saito, S. Nishino, and H. Matsunami, Fabrication of Inversion-Type n-Channel MOSFET's Using Cubic-SiC on Si(100), IEEE Electron Dev. Let. EDL-7, 692-693 (1986).

6. K. Furukama, A. Hatano, A. Uemoto, Y. Fujii, K. Nakanishi, M. Shigeta, A. Suzuki, and S. Nakajima, Insulated-Gate and Junction-Gate FET's of CVD-Grown β-SiC, IEEE Electron Dev. Let. EDL-8, 48-49 (1987).

7. J. W. Palmour, H. S. Kong, and R. F. Davis, Characterization of Device Parameters in High-Temperature Metal-Oxide-Semiconductor Field-Effect Transistors in β-SiC Thin Films, J. Appl. Phys. 64, 2168-2177 (1988).

8. K. Shibahara, S. Nishino, and H. Matsunami, Metal-Oxide-Semiconductor Characteristics of Chemical Vapor Deposited Cubic-SiC, Jpn. J. Appl. Phys. 23, L862-L864 (1984).

9. R. E. Avila, J. J. Kopanski, and C. D. Fung, Behavior of Inversion Layers in 3C Silicon Carbide, Appl. Phys. Lett. 49, 334-336 (1984).

10. J. J. Kopanski and D. B. Novotny, Electrical Characterization of Beta Silicon Carbide MIS Capacitors with Thermally Grown or Chemical-Vapor-Deposited Oxides, Extended Abstracts of the 176th Electrochemical Society Meeting, Hollywood, Fla, 1989, pp. 722-723.

11. M. I. Chaudhry and W. B. Berry, Passivation of β-SiC Surface with Native and Nonnative Oxides, J. Mater. Res. 4, 1491-1494 (1989).

12. S. M. Tang, W. B. Berry, R. Kwor, M. V. Zeller, and L. G. Matus, High Frequency Capacitance-Voltage Characteristics of Thermally Grown SiO_2 Films on β-SiC, J. Electrochem. Soc. 137, 221-225 (1990).

13. R. C. A. Harris, Metal-Oxide-Semiconductor Capacitors on Silicon Carbide, Solid State Electron. 19, 103-105 (1976).

14. A. Suzuki, H. Ashida, N. Furui, K. Mameno, and H. Matsunami, Thermal Oxidation of SiC and Electrical Properties of Al-SiO_2-SiC MOS Structures, Jpn. J. Appl. Phys. 21, 579-85 (1982).

15. J. J. Kopanski and D. B. Novotny, Development and Characterization of Insulating Layers on Silicon Carbide: Annual Report for February 14, 1988 to February 14, 1989, NISTIR 89-4157 (1989).

16. L. M. Terman, An Investigation of Surface States at a Silicon/Silicon Oxide Interface Employing Metal-Oxide-Silicon Diodes, Solid State Electron. 5, 285-299 (1962).

17. P. S. Winokur, J. R. Schwank, P. J. McWhorter, P. V. Dressendoefer, and D. C. Turpin, Correlating the Radiation Response of MOS Capacitors and Transistors, IEEE Trans. Nucl. Sci. NS-31, 1453-1460 (1984).

18. E. H. Snow, A. S. Grove, B. E. Deal, and C. T. Sah, Ion Transport Phenomena in Insulating Films, J. Appl. Phys. 36, 1664 (1965).

19. M. Lenzlinger and E. H. Snow, Fowler-Nordheim Tunneling in Thermally Grown SiO_2, J. Appl. Phys. 40, 278-283 (1969).

20. E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology (John Wiley & Son, New York, 1982). Discussion of the conductance method in Chapter 5, pp. 176-234.

21. Reference 20, Eq. 5.88, pp. 222-226.

22. Reference 20, p. 186.

23. Reference 20, pp. 207-212.

24. Reference 20, Eq. 5.77, pp. 212-218.

25. Reference 20, p. 197.

26. S. R. Hofstein, Stabilization of MOS Devices, Solid-State Electron. 10, 657-670 (1967).

27. A. K. Sinha and T. E. Smith, Kinetics of the Slow-Trapping Instability at the Si/SiO_2 Interface, J. Electrochem. Soc. 125, 743-746 (1978).

28. D. Lu, G. A. Ruggles, and J. J. Wortman, Effects of Processing Conditions on Negative Bias Temperature Instability in Metal-Oxide-Semiconductor Structures, Appl. Phys. Lett. 52, 1344-1346 (1988).

29. R. Adar, I. Bloom, and Y. Nemirovsky, Slow Trapping Measurements in the InSb-Anodic Oxide Interface, Solid-State Electron. 32, 111-118 (1989).

30. W. Kulisch and R. Kassing, Reduction of the Concentration of Slow Insulator States in SiO_2/InP Metal-Insulator-Semiconductor Structures, J. Vac. Sci. Technol. B 5, 523-529 (1987).

31. J. R. Davis, Instabilities in MOS Devices, Electrocomponent Science Monographs, Vol. 1 (Gordon and Breach Science Publishers, New York, 1981), pp. 93-108.

32. P. J. McWhorter and P. S. Winokur, Simple Technique for Separating the Effects of Interface Traps and Trapped-Oxide Charge in Metal-Oxide-Semiconductor Transistors, Appl. Phys. Lett. 48, 133-135 (1986).

33. S. M. Sze, Physics of Semiconductor Devices (John Wiley & Sons, 1981), p. 403.

34. M. A. Lampert and P. Mark, Current Injection in Solids (Academic Press, New York, 1970).

35. Z. A. Weinberg, On Tunneling in Metal-Oxide-Silicon Structures, J. Appl. Phys. 53, 5052-5056 (1982).

36. R. B. Calligaro, Iterative Determination of Oxide Thickness in MOS Structures from One DC Current/Voltage Pair, Electronics Lett. 20, 70-72 (1984).

37. Z. A. Weinberg, Tunneling of Electrons from Si into Thermally Grown SiO_2, Solid State Technol. 20, 11-18 (1977).

38. M. A. Kadyrov, N. V. Kunina, A. S. Saidov, Kh. A. Shamuratov, L. V. Sharonova, A. Ya. Shik, and Yu. V. Shmartsev, Investigation of Nonideal Si-SiC Heterojunctions, Sov. Phys. Semicond. 14, 942-944 (1980).

39. J. W. Palmour, H. J. Kim, and R. F. Davis, Wet and Dry Oxidation of Single Crystal β-SiC: Kinetics and Interface Characteristics, Mat. Res. Soc. Symp. Proc. 54 (Materials Research Society, 1986), pp. 553-559.

40. D. J. DiMaria and D. W. Dong, High Current Injection into SiO_2 from Si Rich SiO_2 Films and Experimental Applications, J. Appl. Phys. 51, 2722-2735 (1980).

41. Z. A. Weinberg, W. C. Johnson, and M. A. Lampert, High-Field Transport in SiO_2 on Silicon Induced by Corona Charging of the Unmetallized Surface, J. Appl. Phys. 47, 248-255 (1976).

42. D. V. Lang, Deep-Level Transient Spectroscopy: A New Method to Characterize Traps in Semiconductors, J. Appl. Phys. 45, 3023-3032 (1974).

43. K. L. Wang and A. O. Evwaraye, Determination of Interface and Bulk-Trap States of IGFET's using Deep-Level Transient Spectroscopy, J. Appl. Phys. 47, 4574-4577 (1976).

44. K. L. Wang, MOS Interface-State Density Measurements Using Transient Capacitance Spectroscopy, IEEE Trans. Electron Dev. ED-27, 2231-2239 (1980).

45. D. Vuillaume and J. C. Bourgoin, Characterization of Si-SiO_2 Interface States: Comparison between Transient Capacitance and Conductance Techniques, J. Appl. Phys. 58, 2077-2079 (1985).

46. W. Suttrop, G. Pensl, and P. Lanig, Electrical Investigations on the Boron-Acceptor and D-Center in 6H-SiC, (Extended Abstracts of the Electrochemical Society, Hollywood, Fla, 89-2 October 1989) pp. 716-717.

47. D. E. Ioannou, N. A. Papanicolaou, and P. E. Nordquist, The Effect of Heat Treatment on Au Schottky Contacts on Beta-SiC, IEEE Trans. Electron Dev. ED-34, 1694-1699 (1987).

48. M. Zerbst, Relaxation Effects in Semiconductor-Insulator Interfaces, Z. Angew. Phys. 22, 30-33 (1966). See also reference 6, pp. 411-416.

NIST-114A
(REV. 3-89)

U.S. DEPARTMENT OF COMMERCE
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY

BIBLIOGRAPHIC DATA SHEET

1. PUBLICATION OR REPORT NUMBER
NISTIR 4352

2. PERFORMING ORGANIZATION REPORT NUMBER

3. PUBLICATION DATE
JULY 1990

4. TITLE AND SUBTITLE

MIS Capacitor Studies on Silicon Carbide Single Crystals: Final Report for May 8, 1989 to November 8, 1989

5. AUTHOR(S)

J. J. Kopanski

6. PERFORMING ORGANIZATION (IF JOINT OR OTHER THAN NIST, SEE INSTRUCTIONS)

U.S. DEPARTMENT OF COMMERCE
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
GAITHERSBURG, MD 20899

7. CONTRACT/GRANT NUMBER
NASA Lewis No C-30018-M and C-30007-K

8. TYPE OF REPORT AND PERIOD COVERED
Final, 5/8/89-11/8/89

9. SPONSORING ORGANIZATION NAME AND COMPLETE ADDRESS (STREET, CITY, STATE, ZIP)

NASA - Lewis Research Center
Cleveland, Ohio

10. SUPPLEMENTARY NOTES

[ ] DOCUMENT DESCRIBES A COMPUTER PROGRAM; SF-185, FIPS SOFTWARE SUMMARY, IS ATTACHED.

11. ABSTRACT (A 200-WORD OR LESS FACTUAL SUMMARY OF MOST SIGNIFICANT INFORMATION. IF DOCUMENT INCLUDES A SIGNIFICANT BIBLIOGRAPHY OR LITERATURE SURVEY, MENTION IT HERE.)

In this continuation of previous work, cubic SiC metal-insulator-semiconductor (MIS) capacitors with thermally grown or chemical-vapor-deposited (CVD) insulators were characterized by capacitance-voltage (C-V), conductance-voltage (G-V), and current-voltage (I-V) measurements. The purpose of these measurements was to determine the four charge densities commonly present in an MIS capacitor (oxide fixed charge, N_f; interface trap level density, D_{it}; oxide trapped charge, N_{ot}; and mobile ionic charge, N_m) and to determine the stability of the device properties with electric field stress and temperature. It was found that an electric field stress would alter the shape of the SiC MIS capacitor C-V characteristics. A negative voltage stress at room temperature would result in a negative shift of the C-V characteristics, indicating the creation of positive charge in the oxide. A positive voltage stress at room temperature resulted in no detectable shift of the C-V curve. The sense of these shifts in the C-V curves is the same as that observed for the "slow trapping" instability often observed in silicon and other semiconductor-based MIS capacitors. From the shift in the C-V characteristics at the midgap point, it was found that a negative voltage stress could increase N_{ot} by as much at 5×10^{11} cm^{-2}. A voltage stress was also found to increase D_{it} by as much as 25%. The mobile ionic charge density was determined from a series of elevated temperature bias stress measurements. N_m for the capacitors in this study ranged from less than 1×10^{11} to 4×10^{11} cm^{-2}. It was found that increasing the temperature would also change the shape of
(continued on next page)

12. KEY WORDS (6 TO 12 ENTRIES; ALPHABETICAL ORDER; CAPITALIZE ONLY PROPER NAMES; AND SEPARATE KEY WORDS BY SEMICOLONS)

capacitance-voltage measurements; charge injection; conductance-voltage measurements; Fowler-Nordheim tunneling; high temperature electronics; interface traps; MIS capacitor; MOS capacitor stability; oxide traps; silicon carbide; slow trapping instability

13. AVAILABILITY

[X] UNLIMITED

[ ] FOR OFFICIAL DISTRIBUTION. DO NOT RELEASE TO NATIONAL TECHNICAL INFORMATION SERVICE (NTIS).

[ ] ORDER FROM SUPERINTENDENT OF DOCUMENTS, U.S. GOVERNMENT PRINTING OFFICE, WASHINGTON, DC 20402.

[X] ORDER FROM NATIONAL TECHNICAL INFORMATION SERVICE (NTIS), SPRINGFIELD, VA 22161.

14. NUMBER OF PRINTED PAGES
42

15. PRICE
A03

ELECTRONIC FORM

the C-V characteristics, indicating an increase in the number of active interface traps. The resistivity and breakdown field of various insulators on SiC were determined from the I-V characteristics of the capacitors. For capacitors with thermal oxide insulating layers, the average resistivity was about 10^{16} Ω-cm and the average electric breakdown field was 3.3×10^{6} V/cm. Fowler-Nordheim tunneling was identified as the charge conduction mechanism for thermal oxide layers on cubic SiC. The barrier height between n-type SiC and SiO_2 for the tunneling of electrons was determined to be 1.8 ± 0.1 eV by fitting the Fowler-Nordheim formula to the observed I-V curve. Finally, some deep-level transient capacitance measurements were attempted on some of the SiC MIS capacitors and on Au on SiC Schottky diodes. In the conclusions of this report, a comprehensive summary of the electrical properties of cubic SiC MIS capacitors is presented.